REMARKS

This Response responds to the Office Action dated July 30, 2003 in which the Examiner stated that claims 2-19 are allowed and rejected claims 20-21 under 35 U.S.C. § 103.

Claim 20 claims a circuit modification method comprising the steps of: first, determining whether a glitch error is caused in a predetermined wire by an aggressor comprised of one or more other wires. When a glitch error is caused in the predetermined wire by an aggressor, a driving circuit for driving the predetermined wire is replaced with another one having a higher driving ability then the driving circuit.

Through the method of the claimed invention replacing a driving circuit with another one having a higher driving ability, as claimed in claim 20, the claimed invention provides a circuit modification method which decreases the amount of glitch without increasing the number of inserted buffers. The prior art does not show, teach or suggest replacing a driving circuit as claimed in claim 20.

Claims 20-21 were rejected under 35 U.S.C. §103 as being unpatentable over *Young et al.* (U.S. Patent No. 6,378,109).

Applicant respectfully traverses the Examiner's rejection of the claims under 35 U.S.C. §103. The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, it is respectfully requested that the Examiner withdraws the rejection to the claims and allows the claims to issue.

Young et al. appears to disclose methods for designing and fabricating digital integrated circuits, and in particular to simulation and analysis of the circuit design in order

to detect and eliminate excessive electric field stress on gate oxide of the transistors comprising the digital circuits. (Col. 1, lines 16-20) A method is provided for designing an integrated circuit which contains a plurality of signal lines in close proximity, such that capacitive coupling among the signal lines is operable to induce crosstalk on at least one of the signal lines. Parasitics are extracted from a trial layout of the integrated circuit, and the method further comprises the steps of: grouping the plurality of signal lines into a plurality of aggressor groups; pruning the plurality of signal lines to form a plurality of victim signal lines; building a minimum region network for each victim signal line of the plurality of victim signal lines comprising the respective victim signal line, aggressor signal lines associated with the respective victim signal line, and associated parasitics; simulating the operation of each minimum region network to determine an amount of noise induced on each respective victim signal line by the aggressor signal lines associated with the respective victim signal line, and analyzing the simulation results of each minimum region network to determine if a gate oxide integrity (GOI) violation exists. (Col. 2, line 63 through Col. 3, line 14) Selection of potential victims and their associated aggressors is a crucial step in the crosstalk verification methodology which is performed in FindVictims filtering step 711. Pruning efficiency is extremely important to reduce the crosstalk noise computation time, while not missing victims. A concept of grouping is used to perform victim/aggressor selection. A group is defined as a set of signals that could switch at the same time and hence collectively induce a glitch on a victim that is larger than if the aggressors switched at dispersed times. (Col. 9, lines 10-20) Networks having crosstalk noise violations are tabulated in step 750. In response to a detected crosstalk noise

violation, the design of the IC can be modified to eliminate the violation by changing wire spacing or by insertion of repeaters in the victim signal, for example. (Col. 11, lines 57-61)

Thus, *Young et al.* merely discloses eliminating crosstalk noise by a) changing the wire spacing or b) insertion of repeaters in the victim's signal. Nothing in *Young et al.* shows, teaches or suggests replacing a driving circuit as claimed in claim 20. Applicant respectfully traverses the Examiner's statement that replacing a driving circuit with another one having the same function and a higher driving ability may be achieved by changing wire spacing or by inserting buffers/repeaters. Applicant respectfully points out that changing the wire spacing means that the spacing of the wires carrying the signals are placed further apart in order to decrease the amount of interference therebetween. This is not the same as replacing a driving circuit. Furthermore, Applicant respectfully points out that the insertion of buffers/repeaters means that additional circuits are added to the existing circuitry. Therefore, *Young et al.* teaches away from the claimed invention. Applicant respectfully submits that replacing a driving circuit means that the number of buffers to be inserted is not increased. In *Young et al.* the insertion of buffer circuits would increase the number of elements in the circuit. As described in specification of the present invention at the "Description of the Prior Art", an increase in the number of buffers to be inserted means an increase in area and power consumption of the circuit. This is the type of problem to avoid firstly. That is, Young et al. is technology which contains the problem to be solved by the present invention and is a starting point of the present invention. Applicants respectfully submit that changing wire spacing or inserting buffers/repeaters of

Young et al. are completely different from replacing a driving circuit with another one having a higher driving ability as claimed in claim 20.

Since nothing in *Young et al.* shows, teaches or suggests replacing a driving circuit with another one having a higher driving ability as claimed in claim 20, Applicant respectfully requests the Examiner withdraws the rejection to claim 20 under 35 U.S.C. § 103.

Claim 21 depends from claim 20 and recites additional features. It is respectfully submitted that claim 21 would not have been obvious over *Young et al.* within the meaning of 35 U.S.C. § 103 at least for the reasons as set forth above. Therefore, it is respectfully requested that the Examiner withdraws the rejection to claim 21 under 35 U.S.C. § 103.

Thus, it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested. Should the Examiner find that the application is not now in condition for allowance, it is respectfully requested that the Examiner enters this amendment for purposes of appeal.

If for any reason the Examiner feels that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, applicant respectfully petitions for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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